Design and Modeling of 10-Bit 100MS/s Pipelined ADC With 2.5-Bits/Stage

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ABSTRACT

This paper presents a 10-bit pipelined analog-to-digital converter with five-stages to achieve 10-bit resolution. The front-end sample-hold circuit will sample the input signal. The next four stages are similar and consists of 2.5-bit per stage. The first stage after the sample-and-hold circuit requires operational amplifier DC gain requirement too high around 80 dB and the gain-bandwidth (GBW) of 1200 MHz. As the circuit implementation is switched capacitor so the operational amplifier feedback capacitor requires around 0.2 pF considering the thermal noise limit. The second stage operational amplifier DC gain is 80 dB, while GBW of 900 MHz. The third stage operational amplifier have DC gain of 80 dB and GBW of 650 MHz with sampling capacitor of 0.13 pF. The fourth stage also uses 2.5-bit for the quantization. The last stage uses 2-bit Flash ADC with reference voltage of 0.5 V. The ADC can achieve SNDR of 56.8 dB and SNR of 57.9 dB for the signal bandwidth of 50 MHz with input signal amplitude -0.5 dBFs at input frequency of 36 MHz. The signal band shows no harmonic distortion with very high SFDR of 68.2 dB

Keywords: Pipelined ADC, DC Gain, Quantizer, Operational Amplifier, GBW

1. INTRODUCTION

A pipelined ADC are popular for wideband application with moderate to high resolution applications. The pipelined ADC can achieve SNR of 57 dB for the signal bandwidth of 50 MHz. The structure of the pipelined ADC uses four stage each with 2.5-bit per stage and last stage uses 2-bit Flash ADC. The complete ADC modeled and simulated in MATLAB and results are presented. A analog-to-digital converter (ADC) acts as the interface between analog frontend and digital processing unit. The ADC resolution, power consumption, and area are important considerations in the design of an ADC for wearable sensors. The high resolution is necessary to cater for large changes in signal due to body movement. The low power consumption helps to extend the battery life considering the small size of wearable devices. The small area reduces the cost, which makes the sensor affordable. The successive approximation register (SAR) ADC is an ideal candidate for wearable sensors with its moderate accuracy and excellent power performance SAR ADC utilizing charge redistribution strategy that comprise of capacitors array, MOS switches, a comparator and digital logic have shown good process scaling adaptation and energy efficient property, which have been a good choice for medical imaging signals processing system and some aerospace electronics, especially those demanding high resolution and medium to high sampling rate. The SAR ADC architecture is well suitable for large-scale wireless sensor networks and bio-medical applications due to its moderate speed, moderate resolution and very low-power consumption characteristics. The primary sources of power consumption in a SAR ADC are the comparator and charge/discharge of the capacitor array.

The energy dissipation required to charge/discharge the capacitor array is dominated by the switching sequence. The conventional switching sequence is an inefficient procedure and much of energy is wasted on charging and discharging the capacitor array.

This paper describes a 12-bit 100kS/s SAR ADC for biomedical system. Both top-plate sampling technique and VCM-based switching technique are applied to the capacitor digital-to-analog converter (CDAC) to implement a 12-bit SAR ADC with 10-b capacitor array DAC. To enhance the linearity of proposed ADC, thermometer decoder is used in capacitor array DAC. Switching-energy minimization technique, asynchronous control with a low-power delay circuit and true single phase clocking (TSPC) D_FF are also adopted to reduce power consumption. Simulation results show that the proposed ADC achieves the SNDR of 70.97dB, the SDFR of 80.23dB and the ENOB of 11.49b with the CMOS 0.18μm technology. Total power consumption is 11.16μW under the supply voltage of 1.8V at the sampling frequency of 100 kHz. And the figure of merit (FoM) is 38.79fJ/conversion-steps [1].

In this article, we presented a 12-bit 80MS/s low power successive approximation register (SAR)analog to digital converter (ADC) design. A simplified but effective digital calibration scheme was exploited to make the ADC achieve high resolution without sacrificing more silicon area and power efficiency. A modified redundancy technique was also adopted to guarantee the feasibility of the calibration and meantime ease the burden of the reference buffer circuit. The prototype SAR ADC can work up to a sampling rate of 80MS/s with the performance of > 10.5-bit equivalent number of bits (ENOB), < ±1 least significant bit (LSB) differential nonlinearity (DNL) & integrated nonlinearity (INL), while only consuming less than 2mA current from a 1.1V power supply. The calculated figure of merit (FoM) is 17.4 fJ/conversion-step. This makes it a practical and competitive choice for the applications where high dynamic range and low power are simultaneously required, such as portable medical imaging [2].

This paper presents a successive approximation

register analog-to-digital converter (SAR ADC) design for bio-medical applications. An energy-saving switching sequence technique is proposed to achieve low power consumption. The average switching energy of the capacitor array can be reduced by 56% compared to a conventional switching method. The measured signal-to-noise-and-distortion ratios of the ADC is 46.92 dB at 500KS/s sampling rate with an ultra-low power consumption of only 7.75-μW from a 1-V supply voltage. The ADC is fabricated in a 0.18-μm CMOS technology [3]. This work presents an ultra-Low power 10-bit, 1-kS/s SAR ADC for biomedical applications. To achieve the nano-watt range power consumption, an ultra-low-power design technique has been utilized, inflicting maximum simplicity on the ADC architecture and low transistor count. ADC was designed in 180nm CMOS technology with a I-V power supply and a 1-kS/s sampling rate for monitoring bio potential signals. The ADC achieves a signal-to-noise plus-distortion-ratio of 57.16 dB and consumes 43 nW [4]. A microwatt asynchronous successive approximation register (SAR) ADC is presented. The supply voltage of the SAR ADC is decreased to 0.6 V to fit the low voltage and low power requirements of biomedical systems. The tail capacitor of

the DAC array is reused for least significant bit conversion to decrease the total DAC capacitance thus reducing the power. Asynchronous control logic avoids the high frequency clock generator and further reduces the power consumption. The prototype ADC is fabricated with a standard 0.18 µm CMOS technology. Experimental results show that it achieves an ENOB of 8.3 bit at a 300-kS/s sampling rate. Very low power consumption of 3.04 µW is achieved, resulting in a figure of merit of 32 fJ/conv.-step [5].

A 10-bit SAR is modeled for medical imaging application. The model is simulated using SIMSAR to achieve 10-bit resolution at the supply voltage of 1-V with 0.45-V full scale. The SAR analog-to-digital converters (ADCs) are considered as appropriate candidates for use in wireless communication for their power efficiency. It is difficult to drive such a large sampling capacitor with high accuracy in a short sampling time. One method to reduce the total number of capacitors is to use a split capacitor digital-to-analog converter (CDAC) structure, but the total number of capacitors after the reduction still reaches the pF level. The input signal will be sampled by the front-end sample-hold-circuit integrated in the DAC. The modeling and simulation show that the complete SAR ADC can achieve SNR of 56 dB and effect number of bit (ENOB) 9-bit with input signal amplitude 1-Vp-p at frequency 10-MHz with sampling frequency of 150 MS/s [6].

This works presents 10-bit pipelined analog-to-digital converter with five-stages to achieve 10-bit resolution. The front-end sample-hold circuit will sample the input signal. The next four stages are similar and consists of 2.5-bit per stage. The first stage after the sample-and-hold circuit requires operational amplifier DC gain requirement too high around 80 dB and the gain-bandwidth (GBW) of 1200 MHz. As the circuit implementation is switched capacitor so the operational amplifier feedback capacitor requires around 0.2 pF considering the thermal noise limit. The second stage operational amplifier DC gain is 80 dB, while GBW of 900 MHz. The third stage operational amplifier have DC gain of 80 dB and GBW of 650 MHz with sampling capacitor of 0.13 pF. The fourth stage also uses 2.5-bit for the quantization. The last stage uses 2-bit Flash ADC with reference voltage of 0.5 V. The ADC can achieve SNDR of 56.8 dB and SNR of 57.9 dB for the signal bandwidth of 50 MHz with input signal amplitude -0.5 dBFs at input frequency of 36 MHz. The signal band shows no harmonic distortion with very high SFDR of 68.2 dB

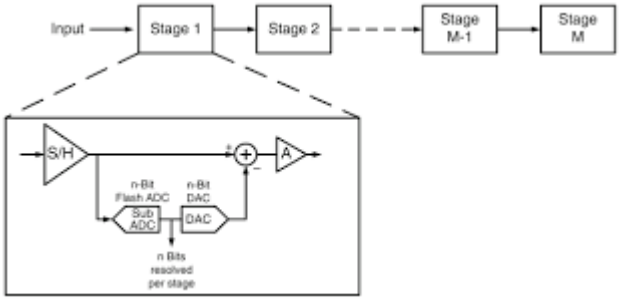
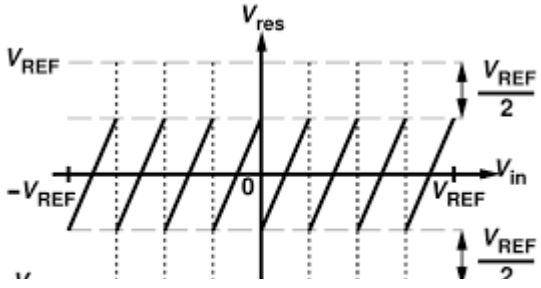


Figure 1: Pipeline ADC Block diagram



After the introduction, the second section discuss the design of the SAR Design, while the third section describes the modeling and simulation of the SAR

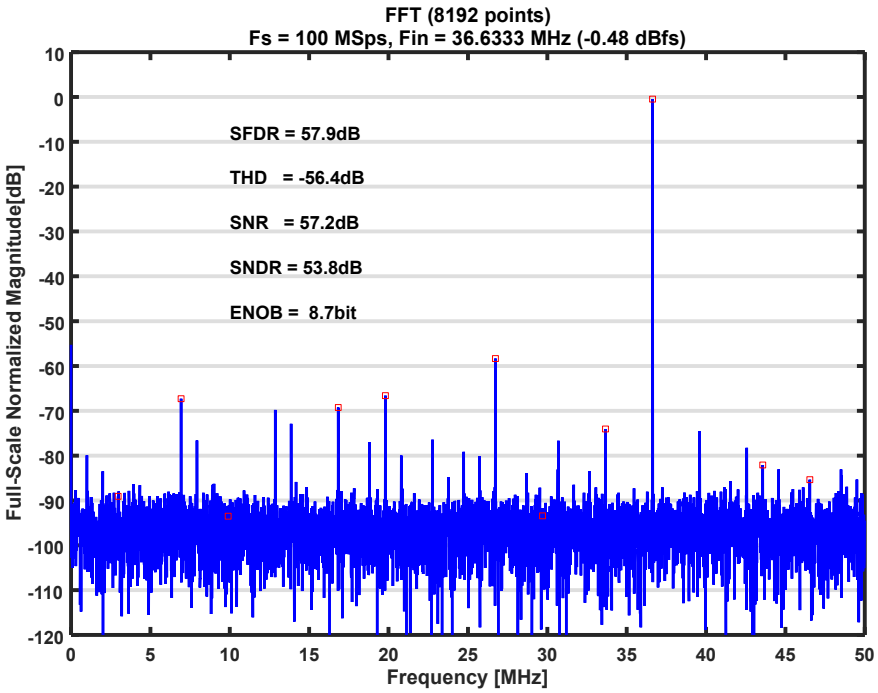


Fig.3: PSD plot for input signal at 36 MHz

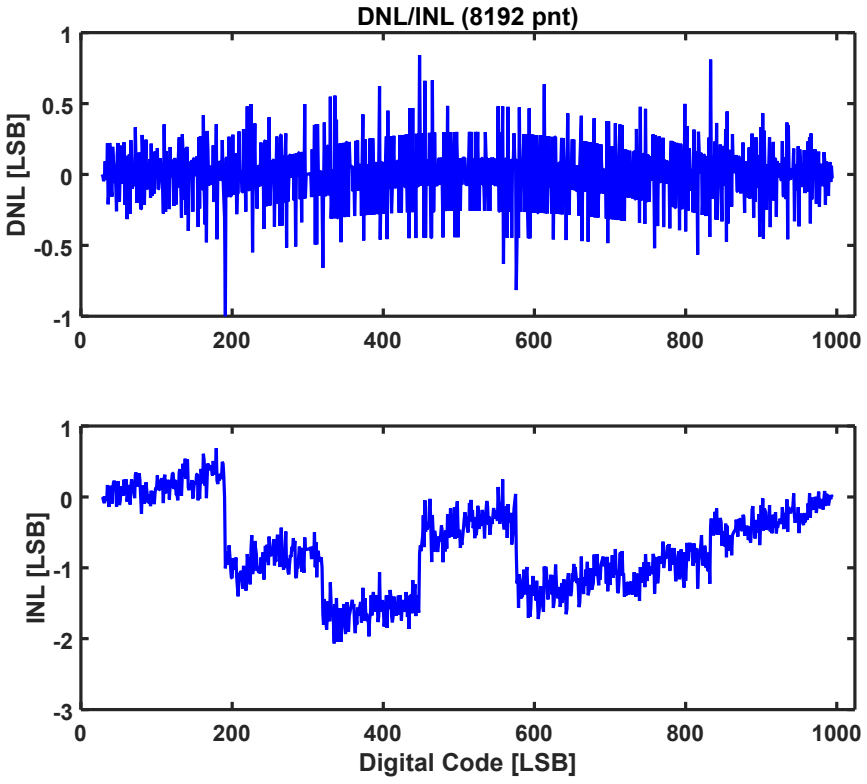


Fig.4: INL/DNL plot for the pipelined ADC

ADC. Finally, the section four concludes the paper.

2. Pipelined ADC DESIGN

A SAR ADC with binary DAC is modeled and simulated using SIMSAR MATLAB environment. A 10-bit DAC implemented using capacitive split-array structure. The integrating DAC implements the sample-&-hold circuit with the split-array DAC. The Figure 1 shows the block diagram of the simulated model of the SAR ADC. The analog building blocks includes a bootstrapped sampling switch, that is at the input sampling. The comparator input had split-array DAC. The analog to digital conversion process completed at the output of the comparator. The DAC implementation uses unit capacitor C of 10 fF. The LSB and MSB DAC array will be divided, and attenuation capacitor will be ratio of LSB and MSB capacitor, which is (32/31) C. The MSB total capacitor is 310 fF, while the LSB total capacitor is 320 fF. The attenuation capacitor will be around 11 fF, which is small. The split array DAC allows to implement 10-bit resolution DAC will much smaller spread of the capacitance. The Figure 2 shows the DAC implementation at the circuit level. The simulated model of ADC can achieve SNR of 56 dB for the signal bandwidth of 75 MHz, with sampling frequency of 150MS/s. The SAR can achieve SNR of 56-dB for signal bandwidth of 75 MHz, with input signal at 10 MHz with amplitude of 1-V_{p-p}. The SNR drop to 28 dB as the full-scale input of the SAR ADC is increased to 1.1-V_{p-p}. The ENOB also drops to 4.4-bit. As the input is further increased the SNR drop more and more. The full-scale input amplitude is increased to 1.2-V_{p-p}, the SNR drop to 22 dB.

4. CONCLUSION

A pipelined ADC with 2.5-bit per stage is modeled and simulated in MATLAB. The topology can achieve SNDR of 56 dB and SNR of 57 dB for signal bandwidth of 50 MHz.

The SAR analog-to-digital converters (ADCs) are considered as appropriate candidates for use in wireless communication for their power efficiency. It is difficult to drive such a large sampling capacitor with high accuracy in a short sampling time. One method to reduce the total number of capacitors is to use a split capacitor digital-to-analog converter (CDAC) structure, but the total number of capacitors after the reduction still reaches the pF level. The input signal will be sampled by the front-end sample-hold-circuit integrated in the DAC. The modeling and simulation show that the complete SAR ADC can achieve SNR of 56 dB and effect number of bit (ENOB) 9-bit with input signal amplitude 1-Vp-p at frequency 10-MHz with sampling frequency of 150 MS/s.

5. ACKNOWLEDGMENT

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